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
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 Hauck, S.;
 Proceedings of the IEEE
 Volume 86, Issue 4, April 1998 Page(s):615 - 638
 Digital Object Identifier 10.1109/5.663540
[AbstractPlus](#) | [References](#) | Full Text: [PDE\(628 KB\)](#) IEEE JNL
- ☐ 2. **Automating the Layout of Reconfigurable Subsystems Using Circuit Generators**
 Phillips, S.; Hauck, S.;
 Field-Programmable Custom Computing Machines, 2005. FCCM 2005. 13th Annual IEEE Symposium on
 18-20 April 2005 Page(s):203 - 212
 Digital Object Identifier 10.1109/FCCM.2005.24
[AbstractPlus](#) | Full Text: [PDE\(304 KB\)](#) IEEE CNF
- ☐ 3. **Programmable active memories: reconfigurable systems come of age**
 Vuillemin, J.E.; Bertin, P.; Roncin, D.; Shand, M.; Touati, H.H.; Boucard, P.;
 Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
 Volume 4, Issue 1, March 1996 Page(s):56 - 69
 Digital Object Identifier 10.1109/92.486081
[AbstractPlus](#) | [References](#) | Full Text: [PDE\(1588 KB\)](#) IEEE JNL
- ☐ 4. **49th Annual Device Research Conference (papers in summary form only received)**
 Electron Devices, IEEE Transactions on
 Volume 38, Issue 12, Dec 1991
 Digital Object Identifier 10.1109/16.158768
[AbstractPlus](#) | Full Text: [PDE\(3996 KB\)](#) IEEE JNL
- ☐ 5. **GANGLION-a fast field-programmable gate array implementation of a connectionist classifier**
 Cox, C.E.; Blanz, W.E.;
 Solid-State Circuits, IEEE Journal of
 Volume 27, Issue 3, March 1992 Page(s):288 - 299
 Digital Object Identifier 10.1109/4.121550
[AbstractPlus](#) | Full Text: [PDE\(1008 KB\)](#) IEEE JNL
- ☐ 6. **Seventh IEEE International Conference on Wafer Scale Integration**
 Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on [see also
 Components, Hybrids, and Manufacturing Technology, IEEE Transactions on]
 Volume 18, Issue 3, Aug 1995
 Digital Object Identifier 10.1109/96.407073
[AbstractPlus](#) | Full Text: [PDE\(4516 KB\)](#) IEEE JNL

-  **7. Cheops: a reconfigurable data-flow system for video processing**
Bove, V.M., Jr.; Watlington, J.A.;
Circuits and Systems for Video Technology, IEEE Transactions on
Volume 5, Issue 2, April 1995 Page(s):140 - 149
Digital Object Identifier 10.1109/76.388062
[AbstractPlus](#) | [Full Text: PDF\(924 KB\)](#) IEEE JNL
-  **8. A wideband all-optical WDM network**
Kaminow, I.P.; Doerr, C.R.; Dragone, C.; Koch, T.; Koren, U.; Saleh, A.A.M.; Kirby, A.J.; Ozveren, C.M.; Schofield, B.;
Thomas, R.E.; Barry, R.A.; Castagnozzi, D.M.; Chan, V.W.S.; Hemenway, B.R., Jr; Marquis, D.; Parikh, S.A.; Stevens,
M.L.; Swanson, E.A.; Finn, S.G.; Gallager, R.G.;
Selected Areas in Communications, IEEE Journal on
Volume 14, Issue 5, June 1996 Page(s):780 - 799
Digital Object Identifier 10.1109/49.510903
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(2244 KB\)](#) IEEE JNL
-  **9. A performance-driven logic emulation system: FPGA network design and performance-driven partitioning**
Chunghee Kim; Hyunchul Shin;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 15, Issue 5, May 1996 Page(s):560 - 568
Digital Object Identifier 10.1109/43.506143
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(888 KB\)](#) IEEE JNL
-  **10. Logic emulation with virtual wires**
Babb, J.; Tessier, R.; Dahl, M.; Hanono, S.Z.; Hoki, D.M.; Agarwal, A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 16, Issue 6, June 1997 Page(s):609 - 626
Digital Object Identifier 10.1109/43.640619
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(520 KB\)](#) IEEE JNL
-  **11. A 2.6-GByte/s multipurpose chip-to-chip interface**
Lau, B.; Yiu-Fai Chan; Moncayo, A.; Ho, J.; Allen, M.; Salmon, J.; Liu, J.; Muthal, M.; Lee, C.; Nguyen, T.; Horine, B.;
Leddige, M.; Kuojim Huang; Wei, J.; Leung Yu; Tarver, R.; Yuwen Hsia; Vu, R.; Tsern, F.; Haw-Jyh Liaw; Hudson, J.;
Nguyen, D.; Donnelly, K.; Crisp, R.;
Solid-State Circuits, IEEE Journal of
Volume 33, Issue 11, Nov. 1998 Page(s):1617 - 1626
Digital Object Identifier 10.1109/4.726545
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(276 KB\)](#) IEEE JNL
-  **12. A flat panel display upgrade solution replaces military CRT technology**
Coker, B.L., Jr.; Willis, M.J.;
Aerospace and Electronic Systems Magazine, IEEE
Volume 13, Issue 10, Oct. 1998 Page(s):33 - 37
Digital Object Identifier 10.1109/62.722418
[AbstractPlus](#) | [Full Text: PDF\(448 KB\)](#) IEEE JNL
-  **13. The Transmogrifier-2: a 1 million gate rapid-prototyping system**
Lewis, D.M.; Galloway, D.R.; Van Ierssel, M.; Rose, J.; Chow, P.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 6, Issue 2, June 1998 Page(s):188 - 198
Digital Object Identifier 10.1109/92.678867
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(192 KB\)](#) IEEE JNL
-  **14. Development of an innovative, two-processor data processing unit for the magnetospheric imaging instrument onboard the Cassini mission to Saturn. I. Hardware architecture**
Psomoulis, A.M.; Cazajus, N.; Dandouras, D.S.; Barthe, H.; Gangloff, M.; Sarris, E.T.;
Geoscience and Remote Sensing, IEEE Transactions on
Volume 37, Issue 4, July 1999 Page(s):1980 - 1996
Digital Object Identifier 10.1109/36.774709
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(716 KB\)](#) IEEE JNL

- ☐ **15. Software radio architecture: a mathematical perspective**
Mitola, J., III;
Selected Areas in Communications, IEEE Journal on
Volume 17, Issue 4, April 1999 Page(s):514 - 538
Digital Object Identifier 10.1109/49.761033
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(464 KB) IEEE JNL
- ☐ **16. PROTEUS-Lite project: dedicated to developing a telecommunication-oriented FPGA and its applications**
Miyazaki, T.; Takahara, A.; Murooka, T.; Katayama, M.; Ichimori, T.; Shirakawa, K.; Tsutsui, A.; Fukami, K.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 8, Issue 4, Aug. 2000 Page(s):401 - 414
Digital Object Identifier 10.1109/92.863619
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(632 KB) IEEE JNL
- ☐ **17. PartGen: a generator of very large circuits to benchmark the partitioning of FPGAs**
Pistorius, J.; Legai, E.; Minoux, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 19, Issue 11, Nov. 2000 Page(s):1314 - 1321
Digital Object Identifier 10.1109/43.892855
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(200 KB) IEEE JNL
- ☐ **18. The 2nd level trigger system of the HADES detector**
Traxler, M.; Becker, R.; Frohlich, I.; Kuhn, W.; Lehnert, J.; Lichtblau, C.; Lins, E.; Petri, M.; Pleier, M.-A.; Ritman, J.;
Nuclear Science, IEEE Transactions on
Volume 47, Issue 2, Part 1, April 2000 Page(s):376 - 380
Digital Object Identifier 10.1109/23.846185
[AbstractPlus](#) | Full Text: [PDF](#)(332 KB) IEEE JNL
- ☐ **19. Prospects for single molecule information processing devices**
Wada, Y.;
Proceedings of the IEEE
Volume 89, Issue 8, Aug. 2001 Page(s):1147 - 1173
Digital Object Identifier 10.1109/5.940278
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(716 KB) | Full Text: [HTML](#) IEEE JNL
- ☐ **20. Subject Index**
Proceedings of the IEEE
Volume 89, Issue 12, Dec. 2001 Page(s):1864 - 1902
Digital Object Identifier 10.1109/JPROC.2001.975951
[AbstractPlus](#) | Full Text: [PDF](#)(282 KB) IEEE JNL
- ☐ **21. A multifunctional processing board for the fast track trigger of the H1 experiment**
Meer, D.; Muller, D.; Muller, J.; Schoning, A.; Wissing, C.;
Nuclear Science, IEEE Transactions on
Volume 49, Issue 2, Part 1, April 2002 Page(s):357 - 361
Digital Object Identifier 10.1109/TNS.2002.1003736
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(235 KB) IEEE JNL
- ☐ **22. Infrastructure IP for configuration and test of boards and systems**
Clark, C.; Ricchetti, M.;
Design & Test of Computers, IEEE
Volume 20, Issue 3, May-June 2003 Page(s):78 - 87
Digital Object Identifier 10.1109/MDT.2003.1198689
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(277 KB) IEEE JNL
- ☐ **23. Programmable Trigger Logic Unit Based on FPGA Technology**
Karstens, F.; Trippel, S.;
Nuclear Science, IEEE Transactions on
Volume 52, Issue 4, Aug. 2005 Page(s):1192 - 1195
Digital Object Identifier 10.1109/TNS.2005.852669
[AbstractPlus](#) | Full Text: [PDF](#)(440 KB) IEEE JNL

**24. Low-power system-on-chip architecture for wireless LANs**

Bisdounis, L.; Dre, C.; Blionas, S.; Metafas, D.; Tatsaki, A.; Ieromnimon, F.; Macii, E.; Rouzet, P.; Zafalon, R.; Benini, L.;
Computers and Digital Techniques, IEE Proceedings-
Volume 151, Issue 1, 15 Jan. 2004 Page(s):2 - 15
Digital Object Identifier 10.1049/ip-cdt:20030978

[AbstractPlus](#) | Full Text: [PDF](#)(1649 KB) IEEE JNL

**25. Reconfigurable Networking Hardware: A Classroom Tool**

Casado, M.; Watson, G.; McKeown, N.;
High Performance Interconnects, 2005. Proceedings. 13th Symposium on
17-19 Aug. 2005 Page(s):151 - 157
Digital Object Identifier 10.1109/CONECT.2005.32

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The roles of FPGAs in reprogrammable systems

Hatuck, S.

Dept. of Electr. Eng. & Comput. Sci., Northwestern Univ., Evanston, IL, USA;

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Abstract:

Reprogrammable systems based on **field programmable gate arrays** are revolutionizing some forms of computation and digital logic. As a logic emulation system, they provide orders of magnitude faster computation than software simulation. As a custom-computing machine, they achieve the highest performance implementation for many types of applications. As a multimode system, they yield significant hardware savings and provide truly generic hardware. In this paper, we discuss the promise and problems of reprogrammable systems. This includes an overview of the chip and system architectures of reprogrammable systems as well as the applications of these systems. We also discuss the challenges and opportunities of future reprogrammable systems

Index Terms

Inspec

Controlled Indexing

field programmable gate arrays **logic design** **reconfigurable architectures**

Non-controlled Indexing

FPGA **chip architecture** **computation** **custom-computing machine** **digital logic** **field programmable gate array**

generic hardware **logic emulation** **multimode system** **reprogrammable system**

Author Keywords

Not Available

References

1. *FPGA Data Book and Design Guide*. Sunnyvale, CA: Actel Corp., 1994.
2. J. K. Adams, H. Schmitt, and D. E. Thomas, "A model and methodology for hardware-software codesign," *Proc. Int. Workshop Hardware-Software Codesign*, 1993.